# **EXOSTIV Dashboard** User's Guide

Rev. 1.0.14 - February 13, 2024





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# **Revision History**

Revision	Modifications
1.0.3	Initial revision
1.0.4	<ul> <li>Added instructions for installing EXOSTIV Dashboard button in Vivado</li> <li>Added menu items description</li> <li>Added Project Archive Manager description</li> <li>Added IP cache controls description</li> <li>Added Design Checkpoint flow description</li> </ul>
1.0.5	<ul> <li>Added RTL flow details</li> <li>Added VCD export details</li> <li>Updated figures</li> </ul>
1.0.6	Minor corrections
1.0.7	Corrected description of timing constraint file usage in RTL flow
1.0.8	Review for EXOSTIV Dashboard for Intel release
1.0.9	<ul> <li>Minor corrections and added the installation procedure (used to be in the Getting Started Guide).</li> </ul>
1.0.10	Added details about the files generated in RTL mode with EXOSTIV for Intel from version     1.8.4
1.0.11	Update usage of generated IP files for EXOSTIV for AMD in RTL mode.
1.0.12	Update of Legal Name and brand names.
1.0.13	Minor modifications in the RTL insertion mode description.
1.0.14	<ul> <li>Updated figures</li> <li>Changed references from Xilinx to AMD</li> <li>Added Exostiv for Microchip</li> <li>Modified legal terms.</li> </ul>



# Introduction

# **Exostiv Dashboard**

This guide provides instructions on how to use the EXOSTIV Dashboard software to extract and visualize debug trace data from FPGA.

For instructions about how to install EXOSTIV Dashboard, refer to Appendix A – EXOSTIV Dashboard Installation Notes.

## **EXOSTIV Dashboard: Main controls**



Connect to EXOSTIV Probe

**EXOSTIV Core Inserter:** use to configure and insert EXOSTIV Probe.

: EXOSTIV Analyzer: use to capture and analyze data from instrumented design.

## **EXOSTIV Dashboard – Welcome screen**

From there, you can create or open a project, access the documentation and manage your software license.



![](_page_5_Picture_0.jpeg)

## **EXOSTIV Dashboard: Menus**

## FILE Menu: EXOSTIV Dashboard-A - D:/Projects File Tools Help New Project Open Project Open Recent Project Save Project Save Project As... Close Project Project Archive Manager Close Search

Please refer to 'Project Archive Manager' below.

Tools Menu:

	EXOSTIV Dashboard-A - D:/Projects/Xplore						
	<u>File Tools H</u> elp						
_	📑 🔗 Connect Device						
-   	Install Dashboard Shortcut						
Ľ	Options						

Please refer to Appendix A – EXOSTIV Dashboard Installation Notes below.

Please refer to Options: interface and project options below

Help Menu:

![](_page_5_Picture_9.jpeg)

Use to manage license and license keys

![](_page_6_Picture_0.jpeg)

## **Options: interface and project options**

This menu item opens the 'Options' dialog that provides general interface and project options.

Option	Description
Vivado	Applies to EXOSTIV for AMD in 'netlist flow'.
Vivado Link Timeout	Sets up the timeout for the 'Vivado Link'. When Vivado
	fails to react to a command from EXOSTIV Dashboard
	after the specified timeout, a dialog opens, prompting
	for cancelling the command or waiting longer.
Capture Units Definition	
EXOSTIV IP Insertion	Sets up the dialog boxes used for confirming actions.
On Application Close	
HDMI Cable Setup	Select to enable output power line on the HDMI cable.
Enable HDMI output power	Please refer to <u>'UG102 - EP Series Connecting Guide'</u> to
	know more about supplying power from the probe onto
	the HDMI cable. This is an advanced feature available
	for use with our MICA board. Please do not enable
	otherwise.
Miscellanous Settings	
Digit grouping	Defines the digit / comma separators for numbers in the
	interface

Options		×
Vivado		
Link with AMD Vivado Timeout	1 minute	$\sim$
Capture Units Definition		
Confirm removing capture unit		
Confirm removing data group		
EXOSTIV IP Insertion		
Allow DRC check		
On Application Close		
Confirm close		
Save wave configuration files		H
save wave comiguration mes		
HDMI Cable Setup		
Enable HDMI output power		
Miscellaneous Settings		
Digit grouping	[	, ~
Restore Defaults Cancel	OK	

![](_page_7_Picture_0.jpeg)

## **Project Archive Manager**

![](_page_7_Picture_2.jpeg)

The 'Project Archive Manager' helps managing, saving and recalling project configurations.

Each generated EXOSTIV IP core has got an 'Universal Unique Identification' ('Uuid') that enables EXOSTIV Dashboard identify an IP once it is inserted inside the target FPGA and check if the settings used in the Dashboard matches it. For instance, EXOSTIV Dashboard must make sure that the capture unit settings match these of the loaded IP before it is able to capture data and properly process it.

If the Uuid of the EXOSTIV IP loaded in the target FPGA does not match the project's Uuid, EXOSTIV Dashboard will refuse to establish a connection with the EXOSTIV IP and won't be able to extract data from the target FPGA.

This ID is defined automatically when the IP is generated.

The Project Archive Manage enables archiving, restoring and deleting project settings. When connecting to an FPGA, it tries to suggest the valid configuration available in the archive that matches the Uuid that is readback from the target instrumented FPGA. It does NOT save and archive the FPGA programming files (bit, bin, sof) generated with the FPGA vendor tool after implementation, which should be managed separately.

![](_page_8_Picture_0.jpeg)

## **Exostiv flows**

EXOSTIV provides 2 user flows – which differ in how the EXOSTIV IP is inserted

1. RTL flow:

In this type of flow, EXOSTIV IP is configured with EXOSTIV Dashboard and provided to the user as a netlist with a component / module top-level in Verilog or VHDL, together with constraint files and possibly additional example files. The insertion into the target design is done at RTL level by the user.

2. Netlist flow:

In this type of flow, EXOSTIV IP is configured with EXOSTIV Dashboard and inserted into the target design after synthesis. EXOSTIV IP is not provided as a separate set of files, but directly integrated into the target design netlist by connecting a list of selected nodes to it.

The figure below provides an overview of the alternative EXOSTIV flows. The Table below sums up the differences between each flow.

![](_page_8_Figure_8.jpeg)

	RTL flow	Netlist flow		
Exostiv for AMD	Available	Available		
Exostiv for Intel	Available	NOT available		
Exostiv for Microchip	Available	NOT available		
Insertion level	RTL (VHDL, Verilog)	Netlist – after synthesis		
Output	Synthesized EXOSTIV IP with RTL (VHDL or	Synthesized & implemented target design including		
	Verilog) wrapper ready to be inserted with	the EXOSTIV IP. Comes with the required constraints.		
	constraints and other configuration files (FPGA			
	family-dependent)			
Remaining steps after	<ul> <li>Manual insertion into target HDL</li> </ul>	- Implementation of instrumented design		
EXOSTIV Core Inserter	code.	(can be run from EXOSTIV Dashboard		
has run	<ul> <li>Synthesis of instrumented design.</li> </ul>	automatically)		
	- Implementation of instrumented	<ul> <li>Binary file generation.</li> </ul>		
	design.	- FPGA programming with binary		
	<ul> <li>FPGA configuration file generation.</li> </ul>	configuration file.		
	- FPGA programming with FPGA			
	vendor configuration file (bin, bit,			
	sof,)			
Level of EXOSTIV IP	The output EXOSTIV IP is set up as a generic IP	EXOSTIV IP is configured and inserted into the target		
configuration	ready to be inserted into the RTL code of the	e design netlist by using a set of queries sent to the		
	target design. The connection of the EXOSTIV	FPGA vendor tool. The nodes that need to be		
	IP with the internal nodes from the target	connected to EXOSTIV IP are selected from the target		
	design is manual. EXOSTIV IP top level provides	s design directly parsed from EXOSTIV Dashboard		
		(using the FPGA vendor tool). After synthesis,		

![](_page_9_Picture_0.jpeg)

a specified number of inputs ready to be	EXOSTIV IP is inserted into the target design netlist
connected.	and automatically connected to the specified nodes
	from the target design.

The user must select the desired IP insertion flow at startup, when creating a new project with EXOSTIV Dashboard.

- EXOSTIV for AMD: Netlist IP Insertion and RTL IP Insertion choices are available
- EXOSTIV for Intel: Only RTL IP Insertion is available.
- EXOSTIV for Microchip: Only RTL IP Insertion is available.

![](_page_9_Picture_6.jpeg)

Name

new\_project

Create in C:/Users/frede

Browse..

Create

Cancel

![](_page_10_Picture_0.jpeg)

# Chapter 1: Core Inserter

## Locate & Start Core Inserter

The Core Inserter opens when creating a new project and when clicking on the Core Inserter icon in the toolbar:

- From the menu: File > New Project:

![](_page_10_Picture_5.jpeg)

EXOSTIV Dasi	hboard-A - D:/Projects/Xplorer/Demo/V( elp	J108/src/epf/q4_g12r156q-1.11.0.epf —
Confi	Link Juration	Capture Configuration
FPGA Type		Connector
Family	Virtex UltraScale	Connector type SFP V
Package	ffva2104	
Speed grade	-2	
Part	xcvu095-ffva2104-2-e	
Search		
Upstream Link		Downstream Link
Transceiver ba	ank 127 🔻	○ Use I2C link
MGT type	GTY	Transceiver bank 127
MGT_TxP0	AK42	MGT_RxP0 AG45
MGT_TxP1	AJ40	MGT_RxP1 AF43
MGT_TxP2	AG40	MGT_RxP2 AE45
MGT_TxP3	AE40	MGT_RxP3 AD43
Reference Clo	ck	Downstream Link Rate
Transceiver ba	ank 127	Line rate division 1
MGT_REFCLK	P0 AF38	Line rate (Gb/s) 12.5
MGT_REFCLK	P1 AD38	Equalization Auto
Frequency (Mi	Hz) 156.25	
	Range : 60 MHz to 650 MHz	
Line rate (Gb/s	s) 12.5	
Link rate (Gb/s	;) 50	
PLL type	QPLL	
PLL type used EXOSTIV clock	QPLL output	
	_	
		Loo Window
Info : EXOSTIV Info : Info : Project f	' Dashboard-A v1.11.0 (Build 231206) ile "D:/Projects/Xplorer/Demo/VCU108/src/ep	/q4_g12r156q-1.11.0.epf* loaded successfully.
list flow [ Link w	ith AMD Vivado 🗰 🛛 EXOSTIV Probe 🗰 🏾	FPGA link 💢

![](_page_11_Picture_0.jpeg)

## **Core Inserter - Overview**

The Core Inserter is made of multiple screens to be used sequentially. This sequential flow is summarized in the top area of the Core Inserter. Clicking in each of the flow steps switches the Dashboard display to a specific page. The top flow bar depends on the chosen EXOSTIV Core Inserter flow (RTL flow or netlist flow).

![](_page_11_Picture_3.jpeg)

Schematically, the following steps must be followed to set up and insert EXOSTIV IP ('Core') in a target design:

#### 1) Link Configuration: sets up the link between EXOSTIV IP and EXOSTIV Probe.

This step is used to define the parameters of the physical link between the target FPGA and EXOSTIV Probe: transceivers parameters, pin locations, type of interface, data rates and so on.

#### 2) Capture Configuration: sets up the capture inside the target FPGA.

This step is used to set up EXOSTIV IP's connections with the internal logic of the target FPGA. It also defines the resources reserved for the IP to sample data, define triggering and filtering events and locally store trace data.

If the 'Netlist IP Insertion flow' is used, a connection with the FPGA vendor design tool is required (currently only applies to EXOSTIV for AMD FPGA).

If the 'RTL IP Insertion flow' is used, this steps is used to define the EXOSTIV IP structure and resources (FIFO size, trigger unit complexity, number of ports, ...)

# 3) **Insert EXOSTIV IP (Netlist flow):** synthesizes EXOSTIV IP, inserts it into target design and run instrumented design implementation.

During this step, EXOSTIV Core Inserter calls the FPGA vendor tool to synthesize EXOSTIV IP, insert it into the target FPGA and connect it to the target FPGA nodes chosen at step 2) and run the implementation of the target design instrumented with EXOSTIV IP.

#### Generate EXOSTIV IP (RTL flow): synthesizes EXOSTIV IP.

During this step, EXOSTIV Core Inserter calls the FPGA vendor tool to synthesize EXOSTIV IP, generate a HDL (VHDL or Verilog) top-level file and constraint files. These files must be used to instrument the target design RTL source code: EXOSTIV IP should then be instantiated into the target code and the instrumented design should be synthesized and implemented with the FPGA vendor tool.

![](_page_12_Picture_0.jpeg)

Once the full core inserter flow is over, the target FPGA can be programmed with the generated programming files (the programming files format depends on the chosen FPGA vendor). Thereafter, EXOSTIV Analyzer can be used to capture data (refer to **Chapter 2: Analyzer**).

## **Core Inserter – Linking to FPGA vendor tool in 'Netlist flow'**

(This section only applies to 'Netlist flow Insertion' - currently only available for AMD FPGA.)

Some of the Core Inserter functionalities - such as selecting the IP connections to the target FPGA nodes or selecting the sampling clock of a capture unit – work based on queries sent by EXOSTIV Dashboard to the FPGA Vendor tool (AMD Vivado). *This link is used in 'Netlist flow'* only.

To use these features, a link must be established between EXOSTIV Dashboard and the FPGA Vendor tool.

To establish a link between EXOSTIV Dashboard and Vivado, please proceed as follows:

- 1. Open Vivado and open the project containing the target FPGA design.
- 2. From the flow navigator in Vivado, open synthesized design or a design checkpoint saved after the synthesis of your design.

If the design was not synthesized, you'll have to synthesize it.

 Click on the 'Open EXOSTIV Dashboard' icon in the toolbar. This shortcut is installed with EXOSTIV Dashboard.
 Can't find it? Refer to Appendix A – EXOSTIV Dashboard Installation Notes

🚴 demo_vcu108 - [D:/Projects/Xplorer/Demo/VCU108/vivado/demo-vcu108-1.10.1-qsfp_2022.1/demo_vcu108.xpr}- Vivado 2022.1										
<u>F</u> ile	<u>E</u> dit	F <u>l</u> ow	<u>T</u> ools	Rep <u>o</u> rts	<u>W</u> indow	Layout	<u>V</u> iew	<u>H</u> elp	Q- Quick Access	
		< \ →		ШX	۰ 🆌	10 H	Ū	¢ ک	Σ 12 1/	× 🗖 🗖 🗖 👘

If you cannot find it, you can install it from the EXOSTIV Dashboard menu: **Tools > Install Dashboard Shortcut** You'll have to shut down Vivado and restart from 1.

4. After clicking on the shortcut, the following window appears, listing the instances of EXOSTIV Dashboard currently running:

EXOSTIV Dashboard Lau	uncher				—		×
Link to Vivado Bring To	Front	ew Dashboard		Location Network $\checkmark$		Query	(
Host Name	IP Address	Local	Pid	Project File			
8PICLT19		yes	12128		(q4_g	12r156q-	1.1

![](_page_13_Picture_0.jpeg)

- 5. Select the desired instance and click on 'Link to Vivado'.
- 6. **Switch back to the EXOSTIV Dashboard**. You are now connected to Vivado with EXOSTIV Dashboard.

![](_page_14_Picture_0.jpeg)

## **Core Inserter – Link Configuration**

## Link Configuration: locate and access

- Click on the 'Link Configuration' button of the top bar of the Core Inserter.

![](_page_14_Figure_4.jpeg)

## Link Configuration: overview

The 'Link Configuration window' is used to configure the interface between EXOSTIV IP and EXOSTIV Probe. It sets up the transceivers. Please refer to <u>UG401 – EXOSITV IP user's guide</u> for a detailed description of the IP's parameters.

## Link Configuration: parameters

![](_page_14_Figure_8.jpeg)

![](_page_15_Picture_0.jpeg)

EXOSTIV Dashboard-A - D:/Projects/Xplorer/Demo/VCU10	//src/epf/q4_g12r156q-1.11.0.epf	- 🗆 X
<u>F</u> ile <u>T</u> ools <u>H</u> elp		
🖸 😑 📬 🔐 🔗 🛠 🕷		
Link Configuration	Capture Insert EXOSTIV IP	Debug Design
FPGA Type	Connector	
Family Virtex UltraScale V	Connector type SFP ~	
Package ffva2104 V		
Speed grade -2 ~		
Part xcvu095-ffva2104-2-e ~		
Search		
Upstream Link	Downstream Link	
Transceiver bank 127 V	○ Use I2C link	
MGT type GTY	Transceiver bank 127	
MGT_TxP0 AK42	MGT RxP0 AG45	
MGT_TxP1 AJ40	MGT_RxP1 AF43	
MGT_TxP2 AG40	MGT_RxP2 AE45	
MGT_TxP3 AE40	MGT_RxP3 AD43	
Reference Clock	Downstream Link Rate	
Transceiver bank 127 V	Line rate division 1 V	
MGT_REFCLK_P0 AF38	Line rate (Gb/s) 12.5	
MGT_REFCLK_P1 AD38	Equalization Auto ~	
Frequency (MHz) 156.25		
Range : 60 MHz to 650 MHz		
Line rate (Gb/s) 12.5 V		
Link rate (Gb/s) 50		
PLL type QPLL V		
EXOSTIV dock output		
<u>و</u>	Log Window	
000		
and a second		
ŭ		
letlist flow 🛛 Link with AMD Vivado 🗰 🗍 EXOSTIV Probe 🗱 🗍 FPG	A link 🗰	

Table 1: Link Configuration parameters

![](_page_16_Picture_0.jpeg)

Control group		Description
control Broad		Description
FPGA Type	FPGA Type	Use these controls to define the target FPGA family, device,
	Family Artix-7	speed grade and package.
	Package csg325	
	Speed grade -2 💌	
	Part xc7a35tcsg325-2 🔻	
	1	
	FPGA Type	
	Family Arria 10 🔻	
	Package NF40	
	Speed grade 3	
	Part 10AX115N4F40I3SGES	
	L	
	FPGA Type	
	Family SmartFusion 2 V	
	Package FC1152 ~	
	Speed grade -1	
	Part M2S150T(S)-1FC1152	
	Search	
	Search	
Connector	Connector	Choose the connector that will be used on the EXOSTIV
	Connector type SFP ~	Probe. Please refer to <u>'UG201 : Interfacing EXOSTIV Probe</u>
		EP Series' Series for more details about the physical
		connection with EXOSTIV Probe.
Upstream link	Linstream Link	Use these controls to set up the 'Upstream link' – that is the
		link between EXOSTIV IP and EXOSTIV Probe. This link uses
		from 1 to 4 transceivers. The transceivers are designated
		from their I/O bank on the FPGA and the I/O site of their 'P'
		channel. Please refer to the chosen FPGA pinout and its
		connections on the target board.
		At IP insertion, there is no restriction on the number of
		transceivers. EXOSTIV Probes have from 1 to 4 usable
		transceivers, depending on the chosen option. Please make
	Upstream link transceivers choice grouped b	sure to generate an EXOSTIV IP that can be used with your
	4 (Quad, AMD FPGA and	* EXOSTIV Probe.
	Microchip FPGA)	
		Transceiver bank: select the I/O bank of the target FPGA
		that is reserved for use with EXOSTIV
	Upstream Link	<b>MGT_TxP#</b> : click on the corresponding tick box to use this
	Transceiver bank 1E	transceiver in EXOSTIV IP. The I/O site for the P pin is
	MGT type GX	derived from the 'transceiver bank' choice above.
	MGT TXP0 AL 37	
	MGT TXP1 AK39	
	MGT TxP2 AJ37	
	MGT TXP3 AH39	
	MGT TxP4 AG37	
	MGT TXP5 AF39	
	Upstream link transceivers choice grouped b	by
	6 (transceivers banks, Intel FPGA)	

![](_page_17_Picture_0.jpeg)

Downstream link	Downstream Link Use I2C link Use I2C link Use transceiver link Transceiver bank I27 MGT_RxP0 AG45 MGT_RxP1 AF43 MGT_RxP2 AE45 MGT_RxP3 AD43	As described in UG401 – EXOSTIV IP user's guide, EXOSTIV IP implements a downstream link that is used to control the IP during analysis (e.g.: to change the trigger condition at runtime.). This downstream link is implemented differently when using the HDMI or the SFP type of connector: - With the SFP type, the downstream link is implemented with the link itself. Once the SFP type is selected, the location of the downstream link transceiver must be specified. - With the HDMI type, 2 extra pins are needed on the FPGA package for a downstream link using a protocol similar to I2C. Once the HDMI type is selected, the location and I/O standard of these pins must be specified.
		Please refer to <u>UG201 : Interfacing EXOSTIV Probe EP Series</u> for a detailed description of the pin allocation and the required physical connections.
Reference clock	Reference Clock         Transceiver bank       127         MGT_REFCLK_P0       AF38         MGT_REFCLK_P1       AD38         Frequency (MHz)       156.25         Line rate (Gb/s)       12.5         Uine rate (Gb/s)       12.5         Uink rate (Gb/s)       50         PLL type       QPLL         EXOSTIV dock output       Image: 60 MHz to 650 MHz         EXOSTIV dock output       Image: 60 MHz to 650 MHz         Reference Clock controls for AMD FPGA         Reference Clock       Image: 70 MHz to 800 MHz         MGT_REFCLK_P0       AE29         Image: 30 MHz to 800 MHz       Range: 30 MHz to 800 MHz         Uine rate (Gb/s)       6.6         Uine rate (Gb/s)       6.6         Uine rate (Gb/s)       26.4         PLL type used       PUL         EXOSTIV dock output       Image: 30 MHz to 800 MHz         Reference Clock controls for Intel FPGA       Image: 30 MHz to 800 MHz         Reference Clock controls for Intel FPGA       Image: 70 MHz         Reference Clock       Image: 70 MHz         Image: 70 MHz       70 MEZ         Image: 70 MHz       70 MEZ         Image: 70 MHz       70 MEZ         Image: 70 MHz	This group of control sets up the transceivers' reference clock. The chosen clock depends on the board design. Specify the location it is taken from and the clock frequency. Based on the specified frequency, the desired data rate (line rate) can be derived. The 'EXOSTIV clock output' tick box is a deprecated functionality that should not be used anymore and will be removed from 2024 software builds.

![](_page_18_Picture_0.jpeg)

## **Core Inserter – Capture Configuration**

## **Capture Configuration: locate and access**

![](_page_18_Figure_3.jpeg)

## **Capture Configuration: overview**

The 'Capture Configuration window' is used to set up the EXOSTIV IP's 'capture' logic. It is used to:

- Define the number of nodes from the target FPGA that will be sampled and observed;
- If netlist mode is used (AMD FPGA only), select the nodes to be observed from the target netlis;
- Define the resources allocated to the EXOSTIV IP to detect a trigger condition, sample data from the target FPGA and to send it outside the FPGA to EXOSTIV Probe.

![](_page_18_Figure_9.jpeg)

## Capture Configuration: adding & configuring Capture Units

A 'Capture Unit' is the logic unit added to the EXOSTIV IP, that takes care about sampling data from the target FPGA and sending it to the EXOSTIV Probe.

Each Capture Unit:

- **is connected to 1 to 16 'Data Group(s)'**. The Data Groups are multiplexed and the user can switch from one data group to another during analysis without
  - having to recompile the EXOSTIV IP. Each Data Group can be connected to up to 2,048 FPGA internal logic nodes.
- uses 1 single clock for sampling data.

This clock is chosen among the clocks available internally in the target FPGA. If EXOSTIV must collect data **from more than one clock domain**, a separate capture unit has to be defined for each clock domain. Multiple capture units can use the same reference clock for sampling data.

includes logic for triggering and data qualification.
 This logic is used to detect the conditions for starting a conturp and for fill

This logic is used to detect the conditions for starting a capture and for filtering the data.

![](_page_19_Picture_0.jpeg)

- **includes one FIFO**, that is used for buffering data before sending to the transceivers. This FIFO is implemented by using blocks of memory from the target FPGA fabric.

EXOSTIV Dashboard-A - D:/Projects/Xplorer/Demo/VCU108/src/epf/q4_g12r156q-1.11.0.epf	– 🗆 ×
Eile Iools Help	
Link Configuration Capture Linsert EXOSTIV IP	Debug Design
Capture units (4 out of max. 16) Patterns	
✓ Patterns Triggering Data	
Counter Trigger unit type Levels / Edges / Comparisons V Fifo depth 1024	~
Sine Bit operations X, 0, 1, R, F, B, N Number of data groups 3 out of max	<. 16
Random Bus operations ==, >, <, >=, <=, <>, in range, out of range Number of data probes 16 out of m	ax. 2048
Vide     Vide     Concerner Warn     Dealer     Vide	
SDI Strance ukličation	
Noise Number of pipes Disabled V	
Double click to add Data Group	
V AXIS_slave Sampling Clock	
Devide did to add Data Group	
AUXE master     Clock frequency (MHz)     (optional, only used for bandwith estimation)	
read_port Capture Unit Status	
Double click to add Data Group	
Double click to add Capture Unit Distraming to probe with 16 probes is possible at maximum frequency 382.8125 MHz	
Capturing in burst to probe is always possible.	
Data groups efficiency	
Counter 100% (16/16)	
Sine 100% (16/16)	
A data y oups are optimizing used.	
Loo Window	
ete ete	
Consc	
Netlet flow [ Link with AMD Woods 🛠 [ EVOCTTV Drobe 🛠 [ EPICA link 🛠	

## To add or remove capture units and/or data groups:

Capture units (4 out of max. 16)	Capture units (4 out of max. 16)
✓ Patterns	✓ Patterns X
Counter Double click here to add a data	Counter
Sine group in this capture unit	Sine
Random	Random
Double click to add Data Group	Double click to add Data Group
SDI	Capture units (4 out of max. 16)
Noise	× Patterne
Double click to add Data Group	Patterns
✓ AXIS_slave	Counter
write port	Sine
Double click to add Data Group	Random 🖌 🗶
Double click here to add a capture unit	Double click to add Data Group
Double click to add Data Group Double click to add Capture Unit	Hover on the Capture Unit or the Data Group and click on the 'X' to remove it. Removing a capture unit also removes the data groups of this capture unit.

![](_page_20_Picture_0.jpeg)

## To set up a capture unit or a data group:

Click on the capture unit or the data group that you wish to set up. The Dashboard controls switch to the selected element's settings page.

'N	etl	ist	Fl	low'	•
		150	•••	000	

Capture units (4 out of max. 16)		Patte	rns			
✓ Patterns Counter Sine	Triggering Trigger unit type Bit operations	Levels / Edges / Comparisons	~	Data Fifo depth	1024	~
Random Double click to add Data Group Y Video	Bus operations Event counter width	==, >, <, >=, <=, <>, in range, out of Disabled	frange V	Number of data groups	16 out of max. 16	
SDI Noise Double click to add Data Group	Storage qualification Number of pipes	Disabled	~			
<ul> <li>AXIS_slave</li> <li>write_port</li> <li>Double click to add Data Group</li> <li>AXIS_master</li> <li>read_port</li> </ul>	Sampling Clock Clock signal <u>u_</u> Clock frequency (MHz) Capture Unit Status	demo/sys_clk (optional, only use	l for band	with estimation)		
Double click to add Data Group Double click to add Capture Unit	Sampling clock	Streaming to probe with 16 probes     Official Capturing in burst to probe is always	is possible ays possibl	e at maximum frequency 3 e.	82.8125 MHz.	
	Data groups efficiency	Counter Sine Random () All data groups are optimally used	100 100 100	% (16 / 16) % (16 / 16) % (16 / 16)		

![](_page_20_Figure_5.jpeg)

![](_page_21_Picture_0.jpeg)

#### 'RTL Flow'

Capture units (2 out of max. 16)	video	
pattern     Data Group 1     Double click to add Data Group     video     Data Group 1     Double click to add Data Group     Double click to add Capture Unit	Triggering     Data       Trigger unit type     Levels / Edges / Comparisons     Pilfo depth       Bit operations     X, 0, 1, R, F, B, N       Bit operations     =->, <, >=, <=, <>, in range, out of range       Event counter width     16       Sequencer Depth     Disabled       Number of pipes     Disabled	×. 16 ax. 2048 5
	Sampling Clock Clock frequency (MHz) 150 Capture Unit Status Sampling dock ① Streaming to probe at 150 MHz is possible with maximum 64 probes. ① Streaming to probe with 46 probes is possible at maximum frequency 153, 125 MHz. ① Capturing in burst to probe is always possible. Data groups efficiency Data Group 1 100% (46 / 46) ① All data groups are optimally used.	

Data Group 1
The RTL flow doesn't require signals to be selected in the user design. Only the number of probes must be defined. Number of nodes currently defined for this capture unit: 46.
TC

![](_page_22_Picture_0.jpeg)

## Capture Unit parameters in 'Netlist flow'

(This section only applies to 'Netlist flow Insertion' – currently only available for AMD FPGA.)

### Table 2: Capture Unit parameters

Control group		Description			
Triggering	Trigger unit type       Levels / Edges / Comparisons ▼         Bit operations       X, 0, 1, R, F, B, N         Bus operations       ==         Counter width       Disabled         Sequencer Depth       Disabled         Storage qualification	<ul> <li>Defines the trigger settings for the selected capture unit.</li> <li>Trigger unit type: use this drop-down list to select between 'Levels / Edges / Comparisons' or 'Levels / Edges' only. This setting sets the complexity of the trigger unit by enabling / disabling 'comparison operators'. 'Levels / Edges / Comparisons' requires more FPGA resources. The available operations are summarized under the drop-down control.</li> <li>Counter width: specifies the width of the events counter (will be available in a future version of the Dashboard).</li> <li>Sequencer depth: specifies the depth of the sequential counter state machine (will be available in a future version of the Storage qualification: use this tick box to enable/disable storage qualification for the selected capture unit. 'Storage qualification' allows defining logic conditions on the capture unit inputs in order to filter the incoming data for capture.</li> <li>Number of pipes: defines the number of pipelining stages placed in each of the data groups paths before the capture unit's multiplexer.</li> </ul>			
Data	Data Fifo depth 2048 Number of data groups 3 out of max. 16 Number of data probes 16 out of max. 2048	<ul> <li>Sets up the Capture Unit FIFO and summarizes the capture unit's size         <ul> <li>Fifo depth: specifies the capture unit's FIFO depth. Selectable values: 1024 to 8192.</li> <li>Number of data groups (informative only) shows the number of data groups defined for this capture unit.</li> <li>Number of data probes (informative only) shows the width of the capture unit in bits. This value is the width of the largest data group connected to the capture unit. It also defines the FIFO width.</li> </ul> </li> </ul>			
Sampling clock	Sampling Clock u_demo/Clk	<ul> <li>Defines the reference clock from the target FPGA design used to sample data with the selected capture unit.</li> <li>If data from more than one clock domain must be sampled, a separate capture unit for each clock domain should be defined.</li> <li>To select this clock from the design loaded in Vivado, link dashboard to Vivado first. Then click on</li></ul>			

![](_page_23_Picture_0.jpeg)

#### Data Group parameters in 'Netlist flow'

(This section only applies to 'Netlist flow Insertion' - currently only available for AMD FPGA.)

Signal Names	Data	Trigger
u_demo/sdi_B[90]	$\checkmark$	
u_demo/sdi_G[90]	$\checkmark$	
u_demo/sdi_R[90]	$\checkmark$	
u_demo/sdi_HBlank	$\checkmark$	
u_demo/sdi_SOF	$\checkmark$	
u_demo/sdi_Valid	$\checkmark$	
u_demo/sdi_VBlank	$\checkmark$	
u_demo/sdi_LN[110]	$\checkmark$	$\checkmark$

Each signal connected to the selected data group can be defined as 'Data only' or 'Data and Trigger' with 2 tick boxes. When defined as 'trigger', this signal can be used to define trigger condition during analysis. Unselecting the 'trigger' option for a signal helps reduce the logic resources required for implementing EXOSTIV IP.

### How to select capture unit clocks and data groups signals?

Defining the Capture Unit's sampling clock and selecting the signals (nodes) connected to a data group requires browsing the target FPGA design. To do this, EXOSTIV Dashboard establishes a link with the FPGA vendor tool (Vivado for AMD FPGAs) and sends queries to it.

Please refer to <u>'Core Inserter – Linking to FPGA vendor tool</u>' to know how to establish this link.

#### To select the Capture Unit's sampling clock:

- 1. Select the desired Capture Unit from the left column.
- 2. Click on in the 'Sampling Clock' controls group. It opens the 'Connect Probes' window, from which you can browse the target FPGA design and select the desired clock signal. Click on 'Done'.

Connect Probes	
Design Hierachy	
✓ vcu108	^
dbg_hub	
✓ u_demo	
> blk_dummy.u_c64_buf	
> blk_dummy.u_sys_buf	
> blk_dummy.u_vid_buf	
cdc_speed	Provice decign
cdc_speed_sel_2	Drowse design
> u_afifo	<b>-</b>
> u_axis	
> u_ck_prog	
> u_ckgen	
> u_color	×
min en 1 👘 en 100	····
Filter Signals Signal filter	Search
Found Signals	Clock Signal
clk_20	u_demo/vid_clk
clk_100	
clk_200	
shared_refclk_div	Colorito de ala ale staval
si570_clk	Selected clock signal
si5328_clk	
sl_iport0[1]	>
sl_iport0_1[1]	
sl_iport0_2[1]	
sys_clk	
vid_clk	
Clock signals list	
1	Cancel Done

![](_page_24_Picture_0.jpeg)

## To select a Data Group's signals:

- 1. Select the desired Data Group from the left hand column
- 2. Click on 'Edit Probes'

Capture units (2 out of max. 16)	Video-HD-SDI		
✓ Capture Unit 1	Edit Probes		
Sine	Signal Names	Data	Trigger
Counter	u demo/cdi BIO 01		
Random	u demo/sdi_G[90]		H
Double click to add Data Group	u_demo/sdi_R[90]		
✓ Capture Unit 2	u_demo/sdi_HBlank		
Video-HD-SDI	u_demo/sdi_SOF		
Double click to add Data Group	u_demo/sdi_Valid		
Double click to add Capture Unit	u_demo/sdi_VBlank u_demo/sdi_LN[110]	$\square$	$\Sigma$

3. In the 'Connect Probes' window, the design loaded in Vivado can be browsed and its internal nodes / signals are listed. Use the window controls to select the signals you wish to insert in the selected Data Group from the selected Capture Unit. Click on 'Done' once you're finished.

Connect Probes		
Design Hierachy		
✓ vcu108		^
dbg_hub		
✓ u_demo		
> blk_dummy.u_c64_buf		
blk_dummy.u_sys_buf	Browco docign	
> blk_dummy.u_vid_buf	browse design	
cdc_speed		
cac_speed_sei_2		
> u ckgen		
> u color		~
	•••	
Filter Signals Signal filter		Search
Found Signals	Data Signals	
CLK_125MHZ_N	u_demo/vid_SOF	
CLK_125MHZ_P	u_demo/vid_VBlank	
CPU_RESET_IBUF	u_demo/vid_HBlank	
CPU_RESET	u_demo/vid_Valid	
GPIO_DIP_SW1	u_demo/vid_LN[110]	
	u_demo/vid_R[90]	
GPIO_DIP_SW2		
GPIO DIP SW3		
GPIO DIP SW3 IBUF		
GPIO_LED_0_LS	Selected signals	
GPIO_LED_0_LS_OBUF	Sciected Signals	
GPIO_LED_1_LS		
GPIO_LED_1_LS_OBUF		
GPIO LED 2 LS	¥	
Number of probes : 46	Cancel	Done

![](_page_25_Picture_0.jpeg)

![](_page_25_Picture_1.jpeg)

The sampling clock and the signals connected to a capture unit should be chosen as part of the same clock domain. If a clock is selected and the chosen signals of a data group are not in the corresponding clock domain, it will result a longer implementation of the EXOSTIV IP in the target design – and likely – a timing error. EXOSTIV Dashboard future releases will include an automatic clock selection from data group signals to facilitate the definition and setup of data groups.

## Capture Unit parameters in 'RTL flow'

Control group				Description
Triggering	Triggering Trigger unit type Bit operations Counter width Sequencer Depth Storage qualification Number of pipes	Levels / Edges / Comparisons           X, 0, 1, R, F, B, N         ==         Disabled         Disabled         Disabled	Defines the	trigger settings for the selected capture unit. Trigger unit type: use this drop-down list to select between 'Levels / Edges / Comparisons' or 'Levels / Edges' only. This setting sets the complexity of the trigger unit by enabling / disabling 'comparison operators'. 'Levels / Edges / Comparisons' requires more FPGA resources. The available operations are summarized under the drop-down control. Counter width: specifies the width of the events counter (will be available in a future version of the Dashboard). Sequencer depth: specifies the depth of the sequential counter state machine (will be available in a future version of the Dashboard). <b>Storage qualification:</b> use this tick box to enable/disable storage qualification for the selected capture unit. 'Storage qualification' allows defining logic conditions on the capture unit inputs in order to filter the incoming data for capture. <b>Number of pipes:</b> defines the number of pipelining stages placed in each of the data groups paths before the capture unit's multiplexer.
Data	Data Fifo depth Number of data groups Number of data probes	1024   3 out of max. 16 16 out of max. 2048 obes 0 out of 16	Sets up the unit's size - - - -	Capture Unit FIFO and summarizes the capture Fifo depth: specifies the capture unit's FIFO depth. Selectable values: 1024 to 8192. Number of data groups: specifies the the number of data groups defined for this capture unit. Number of data probes: specifies the width of the capture unit in bits. This value is the width of the data groups connected to the capture unit. It also defines the FIFO width. Number of data only probes: select the tick box to activate the control. It specifies the number of nodes ('data probes') connected to the capture unit that should be used as 'data only'. In such a case, the IP will feature the specified number of inputs that won't be connected to the capture unit logic for triggering. This option helps saving on the capture unit logic resources when the trigger does not have to be sensitive to all the capture unit's inputs.

![](_page_26_Picture_0.jpeg)

#### Data Group parameters in 'RTL flow'

There are no additional parameters for the data groups. The target design nodes are selected by instantiating the IP in the RTL code. Selecting a data group displays the following message, reminding of the specified total width (number of nodes that can be connected) of the data group.

	Capture units (3 out of max. 16)		Vid-Extended
✓ P	Pattern		
	Cnt	×	The RTL flow doesn't require signals to be selected in the user design.
	Sine		
	Noise		Number of nodes currently defined for this capture unit: 80.
	Double click to add Data Group		
~ v	/ideo		
	SDI		
	Noise		
	Double click to add Data Group		
~ v	/id-Extended		•
	Vid-Extended		
	Double click to add Data Group		
	Double click to add Capture Unit		
<			>

## **Capture Unit status**

Streaming data' is the ability to send data to the Exostiv Probe that exceed the storage reserved in the capture unit FPGA memory. This mode of transfer is selected in the Exostiv Dashboard Analyzer (or the Exostiv Blade client) – the alternative mode being 'burst to probe'.

Data		^
Transfer mode	Stream to Probe	~
Number of captures	100 1 to 4,461	

In a first approach, the capture unit is able to stream data out if the bandwidth required to sample data (sampling frequency x number of bits) is lower or equal to the bandwidth available at the transceivers (SERDES).

However, there are additional parameters that condition this ability, like the internal granularity of the IP, the bandwidth efficiency of the DDR accesses in the Exostiv Probe (or Exostiv Blade), and so on. The following article provides a formal computation: <u>'How many nodes can I sample continuously without creating overflows?'</u>.

Exostiv Dashboard and Exostiv Blade client provide this information in their graphical interface – check the **'Capture Unit Status' section'** in the core inserter. This section is available for all capture units (see picture below).

![](_page_27_Picture_0.jpeg)

Link Configuration	Capture Configuration	Insert EXOSTIV IP	Debug Design
Capture units (4 out of max. 16)		Video	
Patterns Counter	Triggering Trigger unit type	Levels / Edges / Comparisons	Fifo depth 2048 🗸
Random Double click to add Data Group	Bit operations Bus operations Event counter width	X, 0, 1, R, F, B, N ==, >, <, >=, <=, <>, in range, out of range 12 ~ N	Number of data groups         2 out of max. 16           Number of data probes         47 out of max. 2048
Video SDI Noise	Sequencer Depth Storage qualification Number of pipes	Disabled V Disabled V	
Double click to add Data Group	Sampling Clock Clock signal	mo/vid_dk	
AXIS_master read_port Double click to add Data Group	Clock frequency (MHz) 150 Capture Unit Status Sampling clock	(optional, only used for bandwith	estimation)
Double click to add Capture Unit		Streaming to probe at 150 MHz is possible with m     Streaming to probe with 47 probes is possible at     Capturing in burst to probe is always possible.	naximum 256 probes. maximum frequency 382.8125 MHz.
	Data groups efficiency	SDI 97% ( Noise 100% (	(46 / 47) (47 / 47)
		<ul> <li>Data group "SDI" is not optimally used.</li> <li>Consider adding probes to this data group to use</li> </ul>	e the link bandwidth optimally.

For the 'Capture Unit Status' to provide a correct information, the following data is required:

- The width of the capture unit in bits. In 'Netlist insertion mode', this value is automatically computed after the nodes to be observed from the target design are selected. In 'RTL insertion mode', this value is an input field that needs to be speficied when setting up core generation.
- 2. The frequency of the sampling clock. Worth noting, this value is not automatically detected and must be provided. In Exostiv Dashboard, this value is optional; in Exostiv Blade client, this value must be entered. The value must be entered as MHz.

The 'Capture Unit Status' returns the following information:

## 'Sampling clock' subsection.

1. Whether 'streaming' is possible or not at the specified sampling frequency. It also provides the maximum number of bit (max width) of the capture unit to be able to stream at the specified sampling frequency.

For the specified capture unit width, it provides the maximum sampling frequency at which streaming remains possible.

2. It reminds the user that the 'burst to probe' mode remains a valid option, as it uses a flow control mechanism with back pressure to prepare and send bursts of data from a buffer implemented in the target FPGA memory.

## 'Data groups efficiency' subsection

In this section, the tool checks whether all data groups are populated with the specified number of bits. Capture units are generated using the largest of the multipexed data groups connected to it. If a data group is composed of a smaller number of bit, some reserved resources and bandwidth are basically wasted.

![](_page_28_Picture_0.jpeg)

## Core Inserter – Insert EXOSTIV IP (Netlist flow)

(Only applies to 'netlist flow', available for AMD FPGA)

## **Insert EXOSTIV IP: locate and access**

![](_page_28_Figure_4.jpeg)

## **Insert EXOSTIV IP: overview**

The 'Run Insertion window' is used to start the insertion of EXOSTIV IP in the target FPGA design. For that purpose, there must be a link with the FPGA vendor tool (Vivado). To link EXOSTIV Dashboard to Vivado, please refer <u>Core Inserter – Linking to FPGA vendor tool.</u>

The 'Run Insertion window' controls are summarized below:

EXOSTIV Dashboard-A - D:/Projects/Xplorer/Demo/VCU108/src/epf/q4_g12r156q-1.11	1.0.epf — 🗆 🗙
<u>File Tools H</u> elp	
🔁 🧰 📾 🥔 🛠 🔆	
Link Configuration Capture Configuration	Insert Debug Design
Insert EXOSTIV IP	to start the EXOSTIV IP insertion process
Conliguration	
Vivado installation folder	EXOSTIV IP instance name iexi_top
Use IP cache Manage Cache	
Progress Path to	Vivado installation EXOSTIV IP instance name
Checking configuration	
Starting Vivado shell	- · · ·
Creating IO project	-
Generating transceiver sites	· · · ·
Creating debug core project IP cache controls	
Configuring debug core	
Generating memories	· ·
Generating transceivers	
Synthesising debug core	· · ·
Inserting debug core	
Connecting probes	-
☑ Implement design impl_1 ✓	- 💉 🖊 🔤 - 👘
Generate bitstream	
	Flow progress bars
	\ <u></u>
	Log Window
Jimo: received invado query packet (p=192,168,1-45,host=84(LL) 19, pid=13668)     Jimo: Repeived Init to Vivado request.     Info: Received Init to Vivado request.     Info: Acknowledged link to Vivado request.	Optional: start implementation and bitstream generation after synthesis (recommended). Specify the implementation name.
vetlist flow 🛛 Link with AMD Vivado ✔ 🗍 EXOSTIV Probe 🗱 🗍 FPGA link 😫	If not selected, the implementation and bitstream
• • • • • • • • • • • • • • • •	generation will need to be started manually from Vivado.

Schematically, when hitting the 'Insert EXOSTIV IP', EXOSTIV Core Inserter will:

- 1. Synthesize the EXOSTIV IP
- 2. Insert the EXOSTIV IP into the target FPGA design loaded in Vivado
- 3. Run the chosen implementation (if selected)
- 4. Generate the bitstream (if selected).

![](_page_29_Picture_0.jpeg)

## Insert EXOSTIV IP: details about the flow

In this section, we provide more details about each step of the EXOSTIV IP insertion flow.

Checking configuration	Checks if the options chosen for EXOSTIV IP are coherent and complete.
Starting Vivado Shell	Starts a separate Vivado session, that will be used to generate the EXOSTIV IP.
	Requires a Vivado license to be properly installed and available.
Creating IO project	Creates a project and reserves the required transceivers sites.
Generating transceiver sites	
Creating debug core project	Creates a separate project in the new Vivado session, that will be used to generate
	the EXOSTIV IP.
Configuring debug core	Generates the source files for the EXOSTIV IP as configured with the EXOSTIV
	Dashboard Core Inserter.
Generating memories	Generates EXOSTIV IP's memories, used in the capture units.
Generating transceivers	Generates the transceivers required for the EXOSTIV IP.
Synthesizing debug core	Synthesizes EXOSTIV IP.
Inserting debug core	Inserts EXOSTIV IP into the target design netlist.
Connecting probes	Connects the chosen nodes from the target design to the inserted EXOSTIV IP.
Implement design	Runs design implementation with Vivado.
Generate bitstream	Generates programming file with Vivado.

![](_page_30_Picture_0.jpeg)

# Core Inserter – Generate EXOSTIV IP (RTL flow)

## Exostiv Dashboard-A – Generate EXOSTIV IP in RTL flow for AMD FPGA

The 'Generate EXOSTIV IP' is available for RTL flow projects only. The 'Generate EXOSTIV IP' window and controls are accessible by clicking on the corresponding button on the flow bar.

EXOSTIV Dashboard-A - C:/Users/frede/new_projectamd.epf			- 🗆 X
<u>File T</u> ools <u>H</u> elp			
🔮 🗰 📬 🚰 🥜 🛠 🔆			
Link Configuration Configuration	$\mathbf{F}$	Generate EXOSTIV IP	Debug Design
Generate EXOSTIV IP	the EXOSTIV IP	generation process	
Configuration	Output		
Vivado installation folder	EXOSTIV IP instan	re name lexi top	i
Use IP cache	Output folder		
Progress		EXOSTIV IP instance name a	ad output folder
Checking configuration	installation		in output loider
Starting Vivado shell		-	
Creating IO project IP cache controls			
Generating transceiver sites		-	
Creating debug core project			
Configuring debug core		-	
Generating memories			
Generating transceivers		-	
Synthesising debug core		-	
Exporting files		-	
			ų <u>/</u> i
		/	
		Flow progress ba	irs
g Info : Replied to Vivado query packet.	Log Window	1.10	^
J Info : Connecting to license server Info : Leased license from server wss://192.168.1.43:44444			
Info : EXOSTIV Dashboard-A v1.11.0 (Build 231206)			
Info : Project file "C:/Users/frede/new_projectamd.epf" written successfully.			
U and the operation of post syn control of post syn control of the syn of the			~
TL flow   Link with AMD Vivado 🗰   EXOSTIV Probe 🗱   FPGA link 🗮			

![](_page_31_Picture_0.jpeg)

📃 EXOSTIV Dashboard-I - C:/Users/frede/new_projectIntel.epf —	$\times$
Eile Iools Help	
📴 🧰 💼 😰 🕜 🛠 🐞	
Link Capture Configuration Capture EXOSTIV IP Debug Design	
Generate EXOSTIV IP Click here to start the EXOSTIV IP generation process	
Configuration Output	
Quartus installation folden D://CAD/ntelFPGA.pro/22.1/quartus/bin54	
Use IP cache Manage Cache Output folder	
Progress	
Checking configuration EXOSTIV IP output name and output folder	
Generating memories IP cache controls	
Configuring debug core -	
Synthesising debug core Dath to Quantus installation folder	
Exporting files -	
Flow progress bars	
	-
A contract of the second secon	
2 Log Window	
8       Info : Failed to create project file 'C:/Program Files/Exostiv Labs/EXOSTIVDashboard-I-1.11.0/new_projectintel.epf''         Info : Failed to open project file 'C:/Program Files/Exostiv Labs/EXOSTIVDashboard-I-1.11.0/new_projectintel.epf''.         Info : FXOSTIV Dashboard-I v1.11.0 (bitld 231206)	
<sup>w</sup> Info :         Project file "C:/Users/firede/new_projectIntel.epf" written successfully. <sup>g</sup> Info : Project file "C:/Users/firede/new_projectIntel.epf" written successfully.             Info : Project file "C:/Users/firede/new_projectIntel.epf" written successfully.	
RTL flow [EXOSTIV Probe 🗱   FPGA link 🗮	<ul> <li></li></ul>

## Exostiv Dashboard-I – Generate EXOSTIV IP in RTL flow for Intel FPGA

![](_page_32_Picture_0.jpeg)

📕 EXOSTIV Dashboard-M - D:/Projects/XplorerM	lic/demo/pattern/impl/m2s150/exostiv/4xSFP_2g500_156m2	5/4xSFP_2g500_156m25_	x.epf		- 🗆 X
<u>F</u> ile <u>T</u> ools <u>H</u> elp					
🔮 💼 📬 😝 🥜 🛠 🕷 👘					
Link Configuration	Capture Configuration	••	Generate EXOSTIV IP	$\mathbf{F}$	Debug Design
Generate EXOSTIV IP	Click here to start the EXOST	IV IP generati	on process		
Configuration	!	Output			
Libero installation folder D:/cad/Microchip/Libero_S	SoC_v2022.2/Designer/bin	EXOSTIV IP instance r	name exi_top		
	i <sup>—</sup>	Output folder	output		
	₹	L			
Progress					
Checking configuration	EXOSTIV	IP output nar	ne and output f	older	
Configuring debug core		•		-	
Generating memories					
Generating transceivers	sceivers Path to Libero installation folder				
Synthesising debug core		Juci		-	
Exporting files				-	
		low progress	bars		- <b>-</b>
	-				
rogging	La	y window			
RTL flow EXOSTIV Probe					

## Exostiv Dashboard-M – Generate EXOSTIV IP in RTL flow for Microchip FPGA

![](_page_33_Picture_0.jpeg)

## Overview of the files generated with the RTL flow

A series of files are generated by the EXOSTIV Dashboard RTL flow IP generation process. These files must be used with the target FPGA design to instrument the target FPGA and use EXOSTIV to debug the FPGA.

![](_page_33_Picture_3.jpeg)

Vendor tools evolution sometimes affect the flow that needs to be applied. For an up-to-date information, please refer to Exostiv Labs knowledge base articles online (links provided in their respective sections below). The information contained in this document reflects the flow to be applied at the date of this document.

Exostiv Dashboard-A (AMD FPGA) Click here: AMD FPGA: RTL flow files usage.

Exostiv Dashboard-I (Intel FPGA) Click here: Intel FPGA: RTL flow files usage.

Exostiv Dashboard-M (Microchip FPGA) Click here: Microchip FPGA: RTL flow files usage.

## **EXOSTIV IP Cache**

The 'EXOSTIV IP Cache' functionality is available for Exostiv Dashboard-A (AMD FPGA) and Exostiv Dashboard-I (Intel FPGA). The EXOSTIV IP Cache controls are accessible from the 'Manage Cache' button on these pages.

Using the EXOSTIV IP Cache is optional: the 'Use IP Cache' option must be selected to enable it.

The EXOSTIV IP Cache enables reusing previously generated EXOSTIV IPs and previously generated memories (RAMs) to skip the EXOSTIV IP synthesis or the EXOSTIV IP memories synthesis.

Using the cache may greatly speed up the process of inserting the EXOSTIV IP, especially when using an incremental debug process.

The button 'Manage Cache' available from the 'Insert EXOSTIV IP' window of the Core Inserter opens a window used to view and delete the contents of the cache.

The cache contents are sorted by:

- 1. Version of FPGA vendor tool software.
- 2. Target FPGA type
- 3. Version of EXOSTIV Dashboard software

It contains:

- 1. Synthesized EXOSTIV IP identified with their UUID.
- 2. The RAMs used with the IP

![](_page_34_Picture_0.jpeg)

![](_page_34_Figure_1.jpeg)

**Deletes the whole IP cache** 

**Deletes the selected element** 

![](_page_35_Picture_0.jpeg)

# Chapter 2: Analyzer

## **Requirements for using the EXOSTIV Dashboard Analyzer**

The EXOSTIV Dashboard 'Analyzer' is the interface used to capture and analyze data from a running FPGA. The Analyzer window is configured to match the objects and settings defined with the EXOSTIV IP. These settings are included in the 'EXOSTIV Dashboard project file' (.epf).

Each EXOSTIV IP generated with the EXOSTIV Dashboard has got a unique identification number. This ID is used when connecting the EXOSTIV Probe to the target FPGA to check if the project that is loaded in the EXOSTIV Dashboard software corresponds to the EXOSTIV IP loaded in the target FPGA.

Hence, here are the cases when EXOSTIV Dashboard Analyzer will not be usable:

- **There is no 'project' defined:** in such a case, there is EXOSTIV IP defined and hence, the probe cannot be connected to the target FPGA. EXOSTIV Dashboard Analyzer does not have any valid setting about the capture units and data sets of the target design.
- **The EXOSTIV IP core has not been synthesized nor implemented in the target FPGA:** in such a case, there may exist some projects settings, but there is no implementation of the target design instrumented with the EXOSTIV IP. EXOSTIV Probe won't be able to connect.
- The project settings have been modified but the EXOSTIV IP core has not been synthesized or there is no implementation of the newly instrumented target FPGA: in such a case, the project does not match the settings of the IP core that is loaded in the FPGA (if any). EXOSTIV Probe won't be able to connect.
  - → Check <u>Chapter 1: Core Inserter</u> to know how to synthesize EXOSTIV IP and implement the instrumented design.
- The project that's loaded in EXOSTIV Dashboard does not match the EXOSTIV IP loaded in the target FPGA: in such a case, the projects settings do not match the IP settings and the Probe won't connect. Therefore, the Analyzer won't be usable.
  - → Please load the target FPGA with the configuration file that corresponds to the active project in EXOSTIV Dashboard.

![](_page_36_Picture_0.jpeg)

![](_page_36_Picture_1.jpeg)

EXOSTIV Dashboard Analyzer provides controls grouped by capture unit. Each Capture Unit has got its own 'tab'.

A capture unit is a functional entity inserted in the EXOSTIV IP that connects to up to 16 multiplexed 'data groups'.

Each data group can count up to 2,048 connections to logic nodes of the target FPGA.

Each capture unit contains logic for defining trigger conditions and – optionally – data qualification conditions. It also contains a memory buffer used as a FIFO.

The figure below shows a general view on EXOSTIV IP. The colored area shows what is controlled from the Dashboard Analyzer at runtime. The other parts are used automatically by the Dashboard software and the probe to change the IP settings and access the captured data at run-time. For detailed information about EXOSTIV IP, please refer to <u>UG401 – EXOSTIV IP</u>.

![](_page_36_Figure_7.jpeg)

![](_page_37_Picture_0.jpeg)

## Capturing data - overview

![](_page_37_Figure_2.jpeg)

#### Typically, capturing data involves defining the following:

- A 'trigger' condition, which is used to detect a logic condition based on the connected FPGA nodes, which defines when data must be recorded.
- A 'Samples per capture' value, which defines the number of samples to be recorded once a trigger condition is detected.
- A 'trigger position' in the capture: it defines the position of the trigger condition in the 'Capture'.
- A 'Number of Captures', which defines the number of such trigger conditions that must be detected to end the capture
  process. A 'capture' ends once it has recorded the required number of samples. Then the capture unit waits until the
  trigger condition is met again and records a new capture. The process repeats until the specified number of captures
  is collected.
- Optionally, a 'data qualification' condition can be defined to filter the captured data. This condition is built as a logic condition on the target FPGA signals connected to the selected capture unit.

## **Capture Unit Selection - Tab organization.**

Each capture unit can be controlled from its own tab. Click on the capture unit tab that you want to control and use.

-	X: 🙊				
	Patterns	Video	AXIS_slave	AXIS_master	
			Data	Group Selection	ו

Each tab provides the following controls, for one single capture unit.

- Data Group Selection: defines the data group to be observed from the selected capture unit.
- Capture Control: defines the way data is captured, the number of samples to capture, the trigger position in the capture and provides status about a running capture. This area also contains the 'START/STOP' buttons used to control a capture and the controls for automatically exporting the waves.
- Trigger and Data Qualification: this whole area is used to define trigger and data qualification conditions for the capture.
- Waveform Viewer: each capture unit tab includes its own waveform viewer to visualize, format and export the captured data.

The settings for one single capture unit are defined from the corresponding tab. To capture data from more than one capture unit, please check 'Multiple Capture Control'.

## **Data Group Selection**

Each Capture Unit can be connected to up to 16 data groups. The **Data Group Selection** drop-down list shows the data groups as defined in the project when setting up EXOSTIV IP with the Dashboard Core Inserter (please refer to <u>Chapter 1: Core Inserter</u>).

This control changes the settings of the IP in the target FPGA so data from the selected data group of the selected capture unit can be captured. The selection can be done for each capture unit.

In RTL flow, the 'Data Group Selection' area features an additional button 'Edit Probes' (see picture below).

![](_page_38_Picture_0.jpeg)

pattern video	
Da	ta Group Selection
Data Group 1	Edit Probes
4	

Edit Probes button: allows remapping the names of data probes

#### Clicking on this button opens the 'Data Probes Remapping' window (see below).

Data Pr	obes R	lemapping			?
				Data Probes Remapping	
attern	vide	20			
Data Gr	oup Pro	obes Remapping —			
✓ Da	ata Gro	oup 1			
		Туре	Offset	Name	Width
	1	Trigger	0	cu1_dg0_Trig[0]	1
	2	Trigger	1	cu1_dg0_Trig[1]	1
	3	Trigger	2	cu1_dg0_Trig[2]	1
	4	Trigger	3	cu1_dg0_Trig[3]	1
	5	Trigger	154	cu1_dg0_Trig[4][110]	12
	6	Data	2516	cu1_dg0_Data[0][90]	10
	7	Data	3526	cu1_dg0_Data[10][90]	10
	8	Data	4536	cu1_dg0_Data[20][90]	10
ct one o	or more	probes, to make b	ousses, split busse	s or rename probes.	
lake Bus	S	Split Bus	Rename	Restore	Cancel Done

Formally, the EXOSTIV IP created with the RTL flow is a generic IP with generic ports called 'cui\_Trig[range]' for data/trig ports and or cuj\_Data[range] for data only ports. When using EXOSTIV Analyzer, it is desirable to rename or regroup these inputs to ease the interpretation of the waves.

This window provides the following functionalities:

- Data Probes renaming
- Data Probes regrouping into bus
- Bus splitting

To rename data probe: double-click on the chose probe in the 'name' column. The name can then be edited.

5	Trigger	4	cu0_Trig[0][4]	1	
6	Trigger	5	cu0_Trig[0][5]	1	
7	Trigger	6	cu0_Trig[0][6]	1	

![](_page_39_Picture_0.jpeg)

To regroup multiple probes into a bus: Hold SHIFT or CTRL and select the probes to regroup by click on them, then click on 'Make Bus' button or right-click to open the contextual menu, and click on 'Make Bus'.

ttern	Video	Vid-Extended			11 5	
Data Gro	up Probe	s Remapping				
✓ Cnt	t					
		Туре	Offset		Name	Width
	1	Trigger	0	cu0_Trig[0][0	]	1
	2	Trigger	1	cu0_Trig[0][1	]	1
	3	Trigger	2	cu0_Trig[0][2	]	1
	4	Trigger	3	cu0_Trig[0][3	]	1
	5	Trigger	4	cu0_Trig[0][4	]	1
	6	Trigger	5	cu0_Trig[0][5	]	1
	7	Trigger	6	cu0_Trig[01[6	1	1
	8	Trigger		cu0_Trig	Make Bus	1
	9	Trigger	8	cu0_Trig	Split Bus	1
	10	Trigger		cu0_Trig	Rename	1
	11	Trigger		cu0_Trig	Restore	1
	12	Trigger	11	cu0_Trig <mark>lan</mark>		1
	13	Trigger	12	cu0_Trig[0][1	2]	1
	14	Trigger	13	cu0_Trig[0][1	3]	1
	15	Trigger	14	cu0_Trig[0][1	4]	1
	16	Trigger	15	cu0_Trig[0][1	5]	1
> Sin > No	e ise					

To split an existing bus while keeping its name: select the bus and click on 'Split Bus' – or select the bus, right click and select 'Split Bus' from the contextual menu.

To restore probes to their original names and grouping: select them and click on 'Restore' – or select them, right click and select 'Restore' from the contextual menu.

The changes are reflected into the waveform window at the next capture. Hence, it is preferable to first define the probe names and grouping, and then proceed with capture.

![](_page_40_Picture_0.jpeg)

# **Capture Control**

accerno maco A		
	Data Group Selection	
		Ť
	Canture Control	
itatus	Capture Control	
Status		
Capture		
	-	
Capture sample	-	
)ata		
	Channe to Darks	
Number of conturos	230 1 to 6 000	~
Samples per captures	1024	
Samples per capture	37888 2.048 to 812.544	
Manual data download		
rigger & Qualificat		
Trigger position	22988 2 to 37,886	
Trigger counter	1 to 4,096	
Qualification counter	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Auto Export Captur	res	
Enable auto export	$\square$	
Disable wave viewer		
Output folder		
Output folder File name		
Output folder File name File handling	Overwrite existing files	~
Output folder File name File handling File format	Overwrite existing files Comma Separated Value	~

![](_page_41_Picture_0.jpeg)

Control	Effect / Action				
Run with trigger	Runs the capture taking all the defined settings into account: transfer mode, number of captures, samples per capture, trigger position, trigger & data qualification conditions.				
Run immediately	Runs a single capture of the length defined by the 'samples per captures'. The trigger and data qualification settings are ignored.				
Stop	Stops (interrupts) a running already captured are uploade	capture. When stopped, the data that has been ed and displayed for processing.			
Connect Probe	Attempts to detect and connected the workstation.	ect to an EXOSTIV Probe present on the USB port of			
Manual data download	Available when the 'manual of the user to download of data	lata download' option tick box is selected. Enables from the probe memory to the PC.			
<u>Status</u> : progress bars with th	e number of captures and the c	collected samples in the running capture.			
<u>Data</u>					
Transfer mode	Burst to Probe	In this mode, data is transferred by bursts whose size do not exceed the size of the FIFO implemented in the capture unit. This mode does not involve 'streaming' data to the EXOSTIV Probe.			
	Stream to Probe	In this mode, data is transferred by bursts whose size is bigger than the size of the FIFO implemented in the capture unit. This mode involves 'streaming' data over the transceivers. Hence, it could generate 'overflows' if the bandwidth required to stream the data exceeds what's available on the gigabit transceivers. For more details, please refer to the following articles in the knowledge base: <u>'How do I know if my capture unit is able to stream data'?</u> And: <u>'How many nodes can I stream continuously</u> without creating overflows?' Or refer to <b>'Capture Unit Status'</b> in the core inserter section of this guide.			
Number of captures	1 to a maximum computed automatically.	Defines the number of captures of size defined by the 'Samples per capture'. The range next to the control helps compute the possible values. This range is based on the total memory available in the probe, the transfer mode and the number of defined capture units and the number of samples per capture.			
Samples per capture (top	32 to the capture unit's	Defines the size of each capture in 'Burst to			
control – drop down list)	FIFO length by steps of power of 2.	Probe' mode. The range next to the control helps compute the possible values.			
Samples per capture (bottom control)	Capture unit's FIFO length to a maximum computed automatically, by steps of 512 (auto rounded to closest upper value).	Defines the size of each capture in 'Streaming to Probe' mode. The range next to the control helps compute the possible values.			
Manual data download	Tick box	When selected, this option disables the automatic transfer of data from the probe memory to the PC. Only the data transferred			

![](_page_42_Picture_0.jpeg)

Control	Effect / Action			
		manually by clicking onto the button is transferred to the PC.		
Trigger & Qualification				
Trigger position	2 to Samples per capture-2	Defines the position of the trigger in each capture. The value specifies a sample number.		
Trigger counter	1 to max value of the counter	Allows triggering on specific (counted) trigger events only. Requires the insertion of the trigger counter during the core insertion.		
Qualification counter	1 to max value of the counter	Allows triggering on specific (counted) qualification events only. Requires the insertion of the trigger counter during the core insertion.		
Auto-export captures: us	e these controls to export data	automatically when it is collected.		
Enable auto export	Enabled / Disabled	Select to enable auto export of the data to a file		
Disable wave viewer		Select if you do not want to encode the captured data in the waveform viewer format. In such a case, data won't be displayed in the waveform viewer		
Output folder		Use to specify the output folder where files should be exported.		
File name		Use to specify the exported file name.		
File handling	Overwrite or	Defines the desired behavior when exporting the		
	Add timestamp	data to files.		
File format	Binary or Comma Separated value	Defines the file format: binary (header + binary data) or CSV file.		
Radix	Binary, Hexadecimal or Unsigned decimal integer	Defines the number format for the exported data.		

![](_page_43_Picture_0.jpeg)

# **Trigger & Data Qualification**

## **Trigger & Data Qualification: overview**

The trigger & data qualification controls are split into 2 areas, as described in the figure below.

The trigger and the data qualification conditions are based on the definition of the following:

- One AND equation: it specifies a set of conditions on the capture unit's signals combined as a logic AND.
- One OR equation: it specifies a set of conditions on the capture unit's signals combined as a logic OR.
- Each equation can use a combination of conditions local to the selected capture unit and the result of the trigger or data qualification from another capture unit.
- The AND and the OR equations described above are combined to form the trigger or the data qualification unit. This combination is defined with the right-hand, as a graphical combination. Please refer to the figure below for an overview of the available paths.

![](_page_43_Picture_9.jpeg)

## Defining Trigger & Data Qualification: usage and rules

Suppose you'd like to modify the AND Equation of the trigger. Please proceed as follows:

1. To add a condition to the list, click on the '+' sign at the top. This opens a window called 'Trigger Signals'.

Trigger Signals	<
u_demo/vid_VBlank u_demo/vid_Valid	
Add Selected Add All Done	

![](_page_44_Picture_0.jpeg)

In this window you can find the list of the signals still available to add a condition to the AND equation.

![](_page_44_Picture_2.jpeg)

This list is composed of the signals from the selected data group connected to the selected capture unit, that are not already used in either the AND or the OR equation. So each signal that is marked as 'trigger' during core insertion (please refer to <u>Core Inserter – Capture Configuration</u>) can be used <u>once</u> in the equations defining the triggers.

- 2. Select the desired signals and click on 'Add Selected'. Or 'Add All'. Then, click on 'Done'. The added signals disappear from the list.
- 3. The AND equation window is completed with the signals we have added:
- 4. Each of the lines in the Equation window is formatted as follows:

3 🗹 u_demo/sdi_LN[110]		!= 🔻	1AF	hex
		1	1	1
Enable or disable condition	Signal name	Operator	Value	Radix

![](_page_45_Picture_0.jpeg)

Control	Description			
Enable / Disable condition	Select to enable condition. Unselect to disable condition.			
Operator	Drop-down list with the available operators: Always available: == : equality != : inequality Only available if Levels/Edges/Comparisons was chosen as an option for 'Trigger unit type' at Core Insertion (refer to <u>Core Inserter – Capture Configuration</u> ) > : greater than < : smaller than >= : greater or equal to <= : smaller or equal to [] : in range ![] : out of range			
Value	Value for combination. Right-click on the fields shows some of the options at bit level. Bit level (binary) possible values: X : don' care 0 : logic 0 1 : logic 1 R : rising edge F : falling edge B: any edge N : no edge Hexadecimal or Decimal values can also be entered if the corresponding radix is chosen (see below).			
Radix	Radix for 'Value'. Right-click to open the menu to change this:			

## **Cross-capture unit trigger**

By default, it is possible to use the result of a trigger condition from one capture unit as a source trigger condition for another capture unit. Because capture units are not always located in the same clock domain, some options are available.

At the bottom of each (AND or OR) equation window, locate the following control 'Use other capture units'. Select tick box to enable it.

![](_page_46_Picture_0.jpeg)

![](_page_46_Picture_1.jpeg)

Click on the 'pencil icon' to edit the options:

A window opens, with the list of the	ne available capture units	(different from the active CU)	:
--------------------------------------	----------------------------	--------------------------------	---

	Trigger	s From Other Capture Units				? ×		
	CII	Capture Unit Name		Enable	Invert	Common Clock		
1	1	Patterns						
2	3	AXIS_slave						
3	4	AXIS_master						
	Enable / Disable usage of this capture unit's trigger condition Optional inverter on the capture unit's trigger condition							
	Select if the capture units share a common clock.							
	Cancel					Done		

Click on 'Done' once set up.

The 'label icon' allows defining a custom logic name for the condition.

Remark about cross-capture unit triggering with multiple clock domains:

When the same sampling clock is used for the capture units, the event sent from the source capture unit to the destination CU is fully synchronous and the detection thereof is immediate. In such a case, it is advised to select the option 'Common clock' so everything remains synchronous.

When the source and destination capture units do not use the same clock the source trigger event is latched into the destination capture unit. Once the event is seen at the output of the latch, the latch is reset. It is important to note that there will be an undefined time between the generation of the source event and its detection at the destination capture unit.

![](_page_47_Picture_0.jpeg)

# Waveform viewer (MYRIAD<sup>™</sup>)

Uideo - Wave Viewer									- 0 ×
					Wave Viewer				
<mark>= २ 💥 🏽 🗄</mark> 💷 ९ (	ଇ୍ପ୍	🔍 🖯 🖨 🔒 🌘	📫 68x 68v ⊖ 🚺	Any transition 🗸 🔅					
u_demo/vid_SOF u_demo/vid_VBlank u_demo/vid_VBlank	0 1	37 20000							<b>(5)</b> -21320 -1E ~
u_demo/vid_Valid • u_demo/vid_LN[110]	0 01F								
▼ u_dema/vid_R[90]	010								
u_demo/vid_R[90][9] u_demo/vid_R[90][8] u_demo/vid_R[90][7]	0 0								
u_dema/vid_R[90][6] u_dema/vid_R[90][6] u_dema/vid_R[90][5]	0 0								
u_demokid_R[9.0][4] u_demokid_R[9.0][3] u_demokid_R[9.0][2] u_demokid_R[9.0][1] u_demokid_R[9.0][0]	10000	1 (1) (1) (1) 1) (1) (1) 1) (1) (1) 1) (1) (1)							
▶ u_demo/vid_G[90]	010								
▶ u_dema^id_8[90]	010								
*		2980000	2010000 3000000	3020003 3046003	3080000 3000	000 3100000 3-	20000 3140000 31	80000 3180000	3206000 3220000 324000
< >	< >	٢	2993288						>

## Features – Overview:

- Dock/Undock window (double-click in title);
- Gigabyte-capable waveform viewer;
- Wave database save / export (CSV, binary, VCD);
- Waves formatting (color, size) Analog or digital display binary, hexadecimal, unsigned;
- Formatting save / recall;
- Flexible and fast zoom, even on very large databases;
- Multi-marker;
- Event and value search;
- Multi-burst display (background color change)
- Burst numbering / special trigger display
- Multi-scale sample count (absolute or within each burst).

# **Multiple Capture Control**

The optionally removable pane of the left-hand side of the Analyzer window provides the controls for running captures from multiple capture units.

The capture settings must be defined for each capture unit separately.

Select the tick box corresponding to the desired Capture Units and use the run with trigger or run controls.

Multiple Capture Control		
H⊧∎3		
Select / Dese	lect all	
Patterns Video AXIS_slave AXIS_master	Idle Done Idle Idle	

![](_page_48_Picture_0.jpeg)

## Status bar

Netlist flow | Link with AMD Vivado 🖌 | EXOSTIV Probe ✔ | FPGA link ✔ | The Status bar returns the connection status of:

- the chosen project flow ('Netlist' or 'RTL').
- the connection between Vivado and EXOSTIV Dashboard if the netlist flow is used.
- the EXOSTIV Probe with the PC ('EXOSTIV Probe').

- the EXOSTIV Probe with EXOSTIV IP ('FPGA link'). When properly connected, the red 'X' turns to a green 'V'.

![](_page_49_Picture_0.jpeg)

# **Appendix A – EXOSTIV Dashboard Installation Notes**

## Installing EXOSTIV Dashboard – Windows 64 bit

- 1) Download the latest version of EXOSTIV Dashboard: go to: <u>www.exostivlabs.com/download</u> Pick the desired version and register to request the download.
- 2) Unpack the program to start installation. Follow the installation process.

![](_page_49_Picture_5.jpeg)

![](_page_50_Picture_0.jpeg)

## Installing the EXOSTIV Probe USB driver

The EXOSTIV probe requires a USB driver to be installed:

- 1) Connect the EXOSTIV Probe to the PC with the USB cable and power it on.
- 2) If not automatically prompted to install a driver, start Windows' Device Manager and locate the EXOSTIV Probe in the list:

Right-click on 'EXOSTIV Probe' and select 'Update Driver Software...'

🗄 Device Manager	-	×
<u>F</u> ile <u>A</u> ction <u>V</u> iew <u>H</u> elp		
✓ ♣ 8piclt15		 
> 👖 Audio inputs and outputs		
> 🍃 Batteries		
> 📓 Biometric devices		
> 🚯 Bluetooth		
> 💻 Computer		
> Disk drives		
> Las Display adapters		
> WDV/CD-ROM drives		
> M Human Interface Devices		
> Expoards		
Mice and other pointing devices		
Modems		
> Monitors		
🗸 🚍 Network adapters		
😨 Dell Wireless 5550 HSPA+ Mini-Card Network Adapter		
🕎 Intel(R) Centrino(R) Wireless-N 1030		
🕎 LogMeln Hamachi Virtual Ethernet Adapter		
Realtek PCIe GBE Family Controller		
😨 VirtualBox Host-Only Ethernet/Adapter		
VMware Virtual Ethernet Adapter for VMnet1		
VMware Virtual Ethernet Adapter for VMnet8		
> Portable Devices		
> 🗒 Ports (COM & LPT)		
> 🚍 Print queues		
> Processors		
> 📊 Smart card readers		
> Software devices		
> 🔟 Sound, video and game controllers		
> Storage controllers		
> 🛄 System devices		
> Universal Serial Bus controllers		

![](_page_51_Picture_0.jpeg)

	1
🗸 🛐 Other devices	
K EXOSTIV Probe	
🛐 Unknown de	Update Driver Software
> 📃 Portable Devices	Disable
> 🛱 Ports (COM & LF	Uninstall
> 📇 Print queues	
>  Processors	Scan for hardware changes
> 🛓 Smart card reade	Proventing.
> Software devices	Properties
> 👖 Sound, video and ga	ime controllers

		×
÷	Update Driver Software - EXOSTIV Probe	
	How do you want to search for driver software?	
	→ Search automatically for updated driver software	
	for your device, unless you've disabled this feature in your device installation	
	settings.	
	$\rightarrow$ Browse my computer for driver software	
	Locate and install driver software manually.	
		Cancel
		×
~	Update Driver Software - EXOSTIV Probe	
	Durante for this of the second s	
	Browse for driver software on your computer	
	Search for driver software in this location:	
	E:\Program Files (x86)\Exostiv Labs\EXOSTIVDashboard\drivers\x64 🗸 🛛 😽	
	✓ Include subfolders	
	Let me pick from a list of device drivers on my computer This list will show installed driver software compatible with the device, and all driver	
	software in the same category as the device.	

![](_page_52_Picture_0.jpeg)

Select 'Browse my computer for driver software' and specify the right location of the driver.

- For 32 bits windows, the default directory is C:\Program Files\Exostiv Labs\EXOSTIVDashboard\drivers\x86
- For 64 bits windows, the default directory is C:\Program Files (x86)\Exostiv Labs\EXOSTIVDashboard\drivers\x64

		×
~	Update Driver Software - YUGO Systems EXOSTIV Probe	
	Windows has successfully updated your driver software	
	Windows has finished installing the driver software for this device:	
	VUGO Systems EXOSTIV Probe	
	Close	

## Installing the EXOSTIV Dashboard button in Vivado

#### (Applies to EXOSTIV for AMD only)

EXOSTIV for AMD provides a 'netlist flow', that enables EXOSTIV IP insertion after synthesis. This flow requires linking EXOSTIV Dashboard to Vivado using a shortcut to a script in Vivado's toolbar. This shortcut is automatically added at the end of the EXOSTIV Dashboard software installation.

In cases where the installation program fails to locate the Vivado installation properly, it is possible that no button gets inserted in the Vivado toolbar.

Please check your Vivado toolbar. If the EXOSTIV icon is NOT visible, then you have to install it manually:

À der	no_vcu1	08 - [D:/Pi	ojects/X	plorer/Demo,	/VCU108/viva	ado/demo-v	cu108-1	.10.1-qsfp_2	022.1/demo_vcu108.xpr] - Vivado 2022.1
<u>F</u> ile	<u>E</u> dit	F <u>l</u> ow	<u>T</u> ools	Rep <u>o</u> rts	<u>W</u> indow	Layout	<u>V</u> iew	<u>H</u> elp	Q- Quick Access
		* *			۵ 🖌	1	ΰ	Ø 🔅	Σ 🕺 🖉 🖌 🖪 🔳

To install the EXOSTIV Dashboard shortcut into Vivado, please use one of the following procedures:

#### Procedure #1 – Through EXOSTIV Dashboard menu (semi-automatic).

- 1. Close Vivado.
- 2. Start EXOSTIV Dashboard
- 3. Click on the following menu item: Tools > Install Dashboard Shortcut

![](_page_53_Picture_0.jpeg)

📃 EX	📕 EXOSTIV Dashboard-A - D:/Projects/Xplore		
<u>F</u> ile	<u>T</u> ools	<u>H</u> elp	
÷	🔗 Connect Device		
Mul Install Dashboard Shortcut Options		nstall Dashboard Shortcut	
		ptions	

4. You should receive the message: 'Integration with Vivado succeeded'.

## Procedure #2 – Setting it up from Vivado

- 1. Start Vivado
- 2. Click on the following meny item: Tools > Customize Commands > Customize commands...

File Flow	Tools Window Help				
	Run Td Script Compile Simulation Lib <u>r</u> aries Xilinx <u>T</u> d Store				
V	Customize Commands >	ustomize Commands			
Hit on the green '+' button on the upper left corner:					

Custom Commands     Press the +   button to Add Command     Menu name:   Shortcut:   No shortcut   Add   Rung command:   Type a Tcl command here   Define Args   Source Td file:   Toolbar Options   Add to the toolbar   Tgoltip:   Icon file path:   Icon file path:   Icon file path:   Icon file path:	Customize Commands     Configure custom Td menu and toolbar entries.				
Press the +   button to Add Command     Menu name:   Shortcut:   No shortcut   Add   Remove   Image: Command here   Im	Custom Commands	Edit Custom Command			
	<ul> <li>Press the ◆</li> <li>button to Add Command</li> </ul>	Menu name: Shortcut: Run command: Source Tcl file: Toolbar Options Add to the Tooltip: Icon file path:	No shortcut Type a Tcl command here toolbar Apply Reset	Add Remove	

### 4. Type 'EXOSTIV Dashboard' in the dialog that opens. Press ENTER.

![](_page_54_Picture_0.jpeg)

1	Customize Commands	7	×
0	Enter a menu name		
	EXOSTIV Dashboard	1	
c	Press ENTER to add the command, ESC to Cancel	stom Command	
	<ul> <li>Press the ↓</li> <li>button to Add Command</li> </ul>	Menu name:	
	?	OK Canc	el

- Enter the following lines in the main dialog window: 5.
  - Run command: source "C:/Program Files (x86)/Exostiv Labs/EXOSTIVDashboard/vivado\_server.tcl" -notrace -Select 'Add to the toolbar' -
  - -Optionally add the following tooltip: Start EXOSTIV Dashboard
  - Icon file path: C:/Program Files (x86)/Exostiv Labs/EXOSTIVDashboard/Exostiv-icon\_32x32.png

Please replace 'C:/Program Files (x86)/Exostiv Labs/EXOSTIVDashboard' with the alternate path that you used for installing the EXOSTIV Dashboard software.

![](_page_55_Picture_0.jpeg)

## Installing EXOSTIV Dashboard – Linux

1. Please refer to: https://www.exostivlabs.com/exostiv/exostiv-technical-specifications/

to check the supported Linux distributions and versions.

2. **Download** the latest version of EXOSTIV Dashboard: go to: <u>http://www.exostivlabs.com/support/downloads/</u> Pick the desired version and register to request the download.

#### 3. Make the installer executable

In the window manager, right-click on the installer. Select the "Permissions" tab and enable the "Allow executing file as program" checkbox.

800	EXOSTIV	-1.5.1-linux-x64-installer.run Properties
Basic Perr	missions	Open With
Owner:		Me
Access:		Read and write
Group:		dima 💌
Access:		Read and write
Others		
Access:		Read-only 👻
Execute:		Allow executing file as program
Security c	ontext:	unknown

#### 4. Run the installer

Double click on the installer to start the software installation. Click three times on "Forward", then on "Finish".

![](_page_55_Picture_10.jpeg)

![](_page_56_Picture_0.jpeg)

😣 🖨 Setup	
Installation Directory	
Please specify the directory	where EXOSTIV Dashboard will be installed.
Installation Directory [/hom	e/dima/EXOSTIV-1.5.1
InstallBuilder	
	Back Forward Cancel
😣 🖨 Setup	
Ready to Install	<b>\$</b>
-	
Setup is now ready to begin	installing EXOSTIV Dashboard on your computer.
InstallBuilder	Back Forward Cancel
Contractions	
	Completing the EXOSTIV Dashboard Setup Wizard
	Setup has finished installing EXOSTIV Dashboard on your
	computer.
	Back Finish Cancel

At the end of the installation, two new icons appear on the desktop to start and uninstall the application.

![](_page_56_Picture_3.jpeg)

![](_page_57_Picture_0.jpeg)

## Before running the application

EXOSTIV Dashboard requires libusb-1.0-0 to access the probe. Type following command to install libusb:

sudo apt-get install libusb-1.0-0

Enter the administrator password to complete the installation.

Libusb requires administrator privilege to use the USB bus. To remove this limitation, proceed as follows:

- Open file "/lib/udev/rules.d/50-udev-default.rules" in a test editor like gedit with administrator rights.
- Search for the following line in the file:

SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb\_device", MODE="0664"

- Replace with this line:

SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb\_device", MODE="0666"

- Save the file.

## Integration with Vivado

Linking EXOSTIV Dashboard to Vivado for Core Insertion requires using a shortcut to a script in Vivado's toolbar.

In Vivado, open the "Customize Commands..." dialog with Tools > Customize Commands > Customize Commands...

![](_page_57_Picture_15.jpeg)

![](_page_58_Picture_0.jpeg)

- Run command : source "/home/<user>/<EXOSTIV installation directory>/vivado\_server.tcl" -notrace
- Icon file path : /home/<user>/<EXOSTIV installation directory>/Exostiv-icon.png

Replace <user> with the user name. Or adapt the path according to the installation folder. Click on "OK" to validate the changes and close the dialog box.

The newly created custom command should now appear in the menu.

<u>F</u> ile	Flow	<u>T</u> ools <u>W</u> indow <u>H</u> elp			
		<u>R</u> un Tcl Script Compile Simulation Lib <u>r</u> aries			
	$\langle /  $	Xilinx <u>T</u> cl Store			
	VI	C <u>u</u> stomize Commands	۲	<u>C</u> ustomize Commands	
		<u>O</u> ptions		EXOSTIV Dashboard	
A nev	v butt	on will appear in the toolbar.			

 Eile
 Edit
 Flow
 Tools
 Window
 Layout
 Yelle

 <td
 <td

The new menu entry and the new button can now be used to start EXOSTIV Dashboard.

## Using the application from a command prompt

The EXOSTIV Dashboard can be started from a command prompt. First go the install folder, typically "cd ./EXOSTIV-1.5.4" and execute command "./ExostivDashboard.sh".

1	<u> </u>	ustomize Commands			×
Enter a menu name					<u> </u>
`	E	XOSTIV Dashboard			A
ç	Pr	ess ENTER to add the command, ESC to Ca	ancel stom Command		
	+	Press the 🔸	Menu name:		
	+	button to Add Command	Shortcut:	No shortcut	A <u>d</u> d <u>R</u> emove
	÷		Run command:	Type a Tcl command here	Define Args
			○ <u>S</u> ource Tcl file:		
			Toolbar Options		
		:	Add <u>t</u> o the	toolbar	
			T <u>o</u> oltip:		
			Icon file path:	ici.	
				<u>A</u> pply <u>R</u> eset	
	?				OK Cancel

- 6. Enter the following lines in the main dialog window:
  - Run command: source "C:/Program Files (x86)/Exostiv Labs/EXOSTIVDashboard/vivado\_server.tcl" -notrace
  - Select 'Add to the toolbar'
  - Optionally add the following tooltip: Start EXOSTIV Dashboard
  - Icon file path: C:/Program Files (x86)/Exostiv Labs/EXOSTIVDashboard/Exostiv-icon\_32x32.png

Please replace 'C:/Program Files (x86)/Exostiv Labs/EXOSTIVDashboard' with the alternate path that you used for installing the EXOSTIV Dashboard software.

![](_page_59_Picture_0.jpeg)

# Appendix B – Using 'Design Checkpoints' (DCP) flow type

(This section applies to Exostiv Dashboard-A for AMD devices)

## Using Vivado with and without project files (.xpr)

AMD Vivado provides several ways to define and implement FPGAs. The default usage of EXOSTIV implies defining 'projects' files in Vivado (.xpr).

However, in some cases, project files are not used – especially when the target FPGA design is not synthesized with Vivado, but with a third-party EDA synthesis tool.

A very common way of using Vivado is to proceed by successively saving 'Design Checkpoints' (.DCP). Such checkpoints allow saving the state of the implemented design at any point of the flow. By using checkpoints, it is not mandatory to use project files (.xpr). The set of commands that can be used in Vivado differ on whether a project file is used or not.

In this section, we present an alternate flow for using Vivado and EXOSTIV Dashboard without Vivado .xpr project file.

### Flow

- We suppose that Vivado is used with the target FPGA design after synthesis. The synthesized design is loaded into Vivado as a netlist. Hence, the starting point is a design checkpoint (.DCP) saved with Vivado after loading the target FPGA design. We suppose that no Vivado project is defined.
- In the EXOSTIV Dashboard, calling the implementation run is based on the preexistence of a Vivado project file. For this reason, the implementation of the FPGA design instrumented with the EXOSTIV IP cannot be started from EXOSTIV Dashboard. Hence, the option of starting the implementation from the EXOSTIV Dashboard must be de-selected.

Insert EXOSTIV IP     Insert EXOSTIV IP <th>••••</th> <th>Debug Design</th>	••••	Debug Design
	••••	Debug Design
Link       Capture       Insert         Configuration       EXOSTIV IP         puration       Output         installation folder       D:/cad/Xilmx/Nvado/2022.1/bin         cache       Manage Cache         ess       cking configuration         ting Vivado shell       ting IO project	••••	Debug Design
Unk       Capture       Insert         Configuration       EXOSTIV IP         Insert EXOSTIV IP       Output         puration       Output         installation folder       D:/cad/Xilmx/Nvado/2022.1/bin         cache       Manage Cache         ess       cking configuration         ting Vivado shell       sting IO project	• • • •	Debug Design
Insert EXOSTIV IP  uration  installation folder  Cutput  EXOSTIV IP  instance name  exi_top  cache  Manage Cache  cking configuration  ting Vivado shell  sting IO project		
guration o installation folder D:/cad/Xilinx/Vivado/2022.1/bin Output cache Manage Cache  css  cking configuration ting Vivado shell ting IO project		
o installation folder D:/cad/Xiinx/Vivado/2022.1/bin EXOSTIV IP instance name exi_top > cache Manage Cache ess scking configuration ting Vivado shell sting IO project	- - -	
P cache Manage Cache  sss scking configuration ting Vivado shell sting IO project	- - -	
ess cking configuration ting Vivado shell ating IO project	- - -	
cking configuration ting Vivado shell sting IO project		
ting Vivado shell ating IO project		
ating IO project		
erating transceiver sites	-	
ating debug core project	-	
ifiguring debug core	-	
erating memories	-	
erating transceivers	-	
thesising debug core		
erting debug core	-	
inecting probes	-	
Implement design impl_1 v		
Generate bitstream		

![](_page_60_Picture_0.jpeg)

- After loading the synthesized design into Vivado (possibly recalling the corresponding design checkpoint), the EXOSTIV Dashboard can be linked to Vivado with the usual flow (please refer to section starting from 'Core Inserter - Overview').
- Pressing the 'Insert EXOSTIV IP' button from the Insert EXOSTIV IP window of the Core Inserter will start and run the flow up the the 'Design Rules Check'. Thereafter, the result is an 'instrumented synthesized design', that is, the same original design netlist, where a synthesized EXOSTIV IP is inserted and connected to the nodes chosen with the EXOSTIV Core Inserter.
- Save your EXOSTIV Dashboard project file.
- From there, the implementation of this 'instrumented design' must be manually started. Here is how:
  - Switch to the Vivado session where the synthesized design had been loaded originally. The unit 'exi\_top' (EXOSTIV IP top) should be present in the design.

Checkpoint Design * - xc7a35tcsg325-2	
Netlist	? _ 🗆 🗳
🖀 🔄 🖪	
🕅 demo_03_N	
🚊 🔚 Leaf Cells (166)	
• a exi_top (exi_top)	
g_demo[0].u_core (demo_03_core)	
i u_dk (dk_gen)	
u_reset (reset_sync)	
u_shuffle_sync (resync_pipe)	
👜 📲 u_time (TimeBase)	
u_vid_mmcm (clk_video)	
i u_vidrst (reset_sync2)	
2. Successively use the following commands from	n the Vivado command line in
- Opt_design	
<ul> <li>(optionally: power_opt_design)</li> </ul>	

- Place design
- (optionally: phys\_opt\_design)
- Route design
- Write\_bitstream <file name>

#### Please refer to Vivado command line / batch mode user's guide for additional details and options.

3. You can then load the FPGA configuration and use EXOSTIV Analyzer.

![](_page_61_Picture_0.jpeg)

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